PanelLan

ZX Model3 Data Sheet

RISC-V

Version 1.1

Dec.11,2023

Revision history

version	date	Reviser	Revision Notes
V1.0	2023-09-30	youjun.leng	first edition
V1.1	2023-12-11	youjun.leng	Added EPWM and CAP function descriptions

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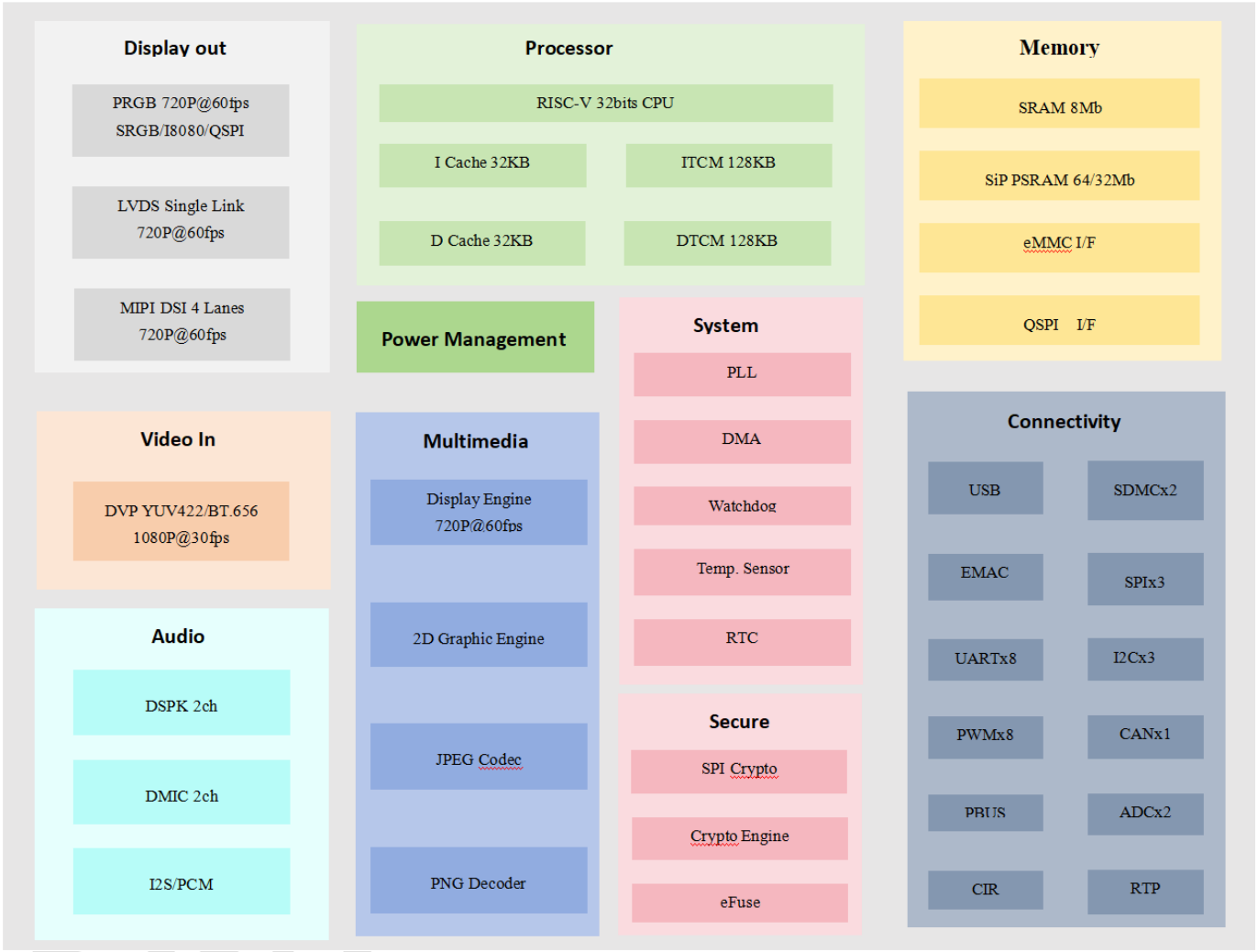
directory

1. Brief introduction

ZX Model3 is a high-performance display interaction and intelligent control MCU, using domestic independent high-computing power RISC-V core, built-in on-chip 1MB large-capacity SRAM and 64Mb PSRAM, and provides rich interconnection peripheral interfaces, equipped with 2D image acceleration engine and PNG decoding/JPEG codec engine, which can meet the needs of various interactive design scenarios and multimedia interaction. With the characteristics of high security and high openness, it can be oriented to pan-industrial applications.

1. 1. Functional block diagram



1. 2. Features

The ZX Model3 series processors are based on the RV32 instruction architecture and have the following features:

1. 2. 1. CPU cores

- Pingtou single-core E907, RV32IMAFDCP instruction architecture, 480MHz@1.1V
- The L1 instruction cache is 32KB and the data cache is 32KB
- Single/double-precision floating-point unit with integrated DSP instruction set
- PMP security protection
- Intra-core interrupt CLINT and interrupt controller CLIC

1.2.2. The system boots

- SD Card(SDMC1)→ SPI NOR → SPI NAND → eMMC(SDMC0)Sequential scans start
- You can change the boot order by flashing eFUSE

1.2.3. System security

- Supports the digitally signed secure boot mode
- CE implements encryption and decryption algorithms such as AES/TDES/RSA and SHA/HMAC digest algorithms
- SPI_ENC SPI NAND/SPI NOR online encryption and decryption
- SID has a built-in fuse 2048bit, of which 512bit is for customer customization
- Built-in 256bit TRNG generator

1.2.4. On-chip storage

- BROM 64KB
- SRAM 1MB, of which 256KB can be configured for TCM use
- PSRAM Specifications:
  - 64Mb, 16-bit width, maximum frequency 200MHz DDR

1.2.5. Storage interfaces

- QSPI In the tank SPI NOR Flash / SPI NAND Flash
  - Support single/dual/quad channel
  - IO max rate SDR 100MHz
  - There is no limit to the Flash capacity
- eMMC4.5/SD3.01/SDIO3.0, 2 sets in total
  - eMMC 4-wire, support SDR25/SDR50/DDR50 mode
  - SD card, support SDR25/SDR50 mode
  - IO max rate DDR 50MHz, only 3.3V IO voltage is supported

1.2.6. Image engine

- DE Display Engine:
  - 1 UI layer, 1 VI layer, up to 720P60
  - VI layers support 1/31.999x ~ 32x scaling
  - Integrated error diffusion Dither algorithm
- GE Image Engine:
  - The maximum input/output image size is 4096x4096
  - Supports both horizontal and vertical Flip, 90/180/270 degree rotation
  - The RGB format supports arbitrary rotation and scan order
  - Support 1/16x ~ 16x scaling, with 6x4 taps 16 phases filtering algorithm
  - Command queues are supported
- VE Video Codec:
  - MJPEG baseline decoder
  - PNG decoder
  - JPEG encoder

1.2.7. Display interface

- Parallel RGB 24bit, maximum performance 720P60
- Single Link LVDS, interface rate up to 700Mbps, maximum performance 720P60

- MIPI DSI 4 LANE, interface rate up to 1Gbps, performance up to 720P60
- Support SRGB/I8080/QSPI screen interface
- DVP 8bit input, pixel clock up to 150MHz, performance up to 1080P30
- The display output interface supports the spread spectrum function

1.2.8. Audio interface

- Left and right digital PWM outputs (DSPK)
- 2-channel DMIC interface input
- 1 set of I2S, support input and output, support TDM mode

1.2.9. Generic interfaces

- 1-way USB, configurable as DEVICE/HOST
- 1 EMAC, supports 100M RMII, supports IEEE1588 protocol
- 4-way SPI, supports 3-wire/4-wire interface, configurable as Master/Slave
- 8-way UART, industry standard 16550 compliant, baud rate accuracy of <2%
- 3-way I2C with 7-bit and 10-bit addressing and up to 400Kb/s
- 1 CAN , support CAN2.0A and CAN2.0B, programmable communication rate up to 1Mbps
- 1 set of CIR, support IR input and IR output
- 1 set of PBUS for read and write access to the external device address space
- 5 GPIOs for a total of 73 IOs, each configured independently:
  - No pull-up/pull-up 33KΩ/pull-down 33KΩ is optional
  - The output drive is adjustable in 8 gears
  - Supports secondary debounce and interrupts
  - Bit operations are supported

1.2.10. counter

- GTC Universal Timer
  - 52-bit timer with system heartbeat clock for a timekeeping period greater than 35 years
  - In debug mode, it can be configured to pause or resume timing
- WDOG Watchdog
  - Support interrupt and reset, timeout time 1ms~37 hours configurable
  - In debug mode, it can be configured to pause or resume timing
  - Hardware write-protection mechanism
- RTC real-time clock
  - In seconds, 100 years time span, hardware alarm clock setting
  - External 32.768KHz crystal, support digital calibration, range ±975ppm
  - Separate backup power input pins for built-in power switching
  - The 128bits register is used for system data backup, such as power-off key protection data
  - The RTC module operates at 2uA
- PWM
  - Built-in 16-bit counter, support 4-way timer
  - It can support up to 8 independent PWMs or 4 complementary PWMs
- EPWM
  - Built-in 16-bit counter, support 12-channel timer
  - It can support up to 24 independent PWMs or 12 complementary PWMs
  - Hardware-triggered ADC sampling is supported
  - It supports the function of outputting a fixed number of pulses
  - The EPWM0-5 supports high-progress PWM with an accuracy of 156ps

- CAP
  - Built-in 32-bit CAP counter, support 6 timers
  - It can support up to 6 channels of signal capture or 6 channels of simple PWM signal output
  - Continuous capture mode or single capture mode is supported

1.2.11. mock

- Built-in 12-channel 12-bit PSADC with a sample rate of up to 2MSPS
- Built-in 8-channel 12-bit GPADC with a sampling rate of up to 2MSPS
- Integrated RTP resistive touchscreen interface

1.2.12. Clock and power management

- The CMU has 4 built-in PLLs:
  - PLL_INT0 for CPU use alone
  - PLL_INT1 Used for buses, internal modules, and low-speed interface modules
  - PLL_FRA0 It is used for storage interface modules and supports spread spectrum
  - PLL_FRA2 It is used for the screen output module and supports spread spectrum
- SYSCFG has 3 built-in LDOs:
  - LDO25 (2.5V 100mA) for system reset startup, ADC power, eFuse power
  - LDO18 (1.8V 100mA) for PSRAM IO and PSRAM particle power
  - LDO1x (0.9~1.9V 500mA, 50mV per step), which can be used for VDD11_SYS power supply
- Built-in THS temperature sensor, support high and low temperature interrupt alarm and over-temperature reset chip

1.3. Product Information

Model	characteristic	encapsulation	Temperature (Tj)
ZX Model 3	1MP SRM + 8MP PSR	QFN88,10x10x0.85mm,0.4mm pitch	-40 to +105°C

1.4. Product comparison

project	ZX Model 3
Encapsulation options	QFN88,10x10mm, 0.4mm pitch
kernel	E907 480MHz @ 1.1V
memory	1MB SRAM 8MB PSRAM
safety	x 1
RGB	x 1
LVDS	x 1
MIPI CIO	x 1

RTP	x 1
DVP	x 1
RTC	x 1
SD3.01	x 1
eMMC4.5/SDIO3.0	x 1
DMIC	x 2
I2S	x 1
CAN	x 1
CIR	x 1
SPK	x 2
SLEEPS	x 4
UART	x 8
I2C	x 3
EMAC-100M	x 1
USB2.0	x 1
PWM	x 4(8hp)
EPWM	x12(24ch)
CAP	x6

2. Electrical characteristics

2. 1. Operating conditions

2. 1. 1. Maximum limit value

sign	description	minimum	maximum	unit
Tstg	Storage temperature	-40	125	℃
VCC33_IO	GPIO power supply	-0.3	3.6	V
RTC_VCOIN	RTC power supply	-0.3	3.6	V
VDD11_SYS	Core and system power supplies	-0.3	1.32	V
Iio	IO input and output current	-55	60	but

2. 1. 2. Recommended operating conditions

sign	description	minimum	Typical	maximum	unit
Tj	Junction temperature	-40		105	℃
Ta	Ambient temperature	-40		85	℃
VCC33_IO	GPIO power	2.7	3.3	3.6	V
RTC_VCOIN	RTC power supply	2.7	3.0	VCC33_IO	V
VDD11_SYS	Core and system power supplies	0.99	1.1	1.21	V

2. 2. RTC power supply

The RTC power supply comes from VCC33_IO and VCOIN, and the internal circuit automatically detects the VCC33_IO and VCOIN voltage, and uses the power supply of the one with the highest voltage.

- When powered on, VCC33_IO is 3.3V, and VCOIN is typically 3.0V for coin cell batteries, so VCC33_IO is used for power supply
- When the VCC33_IO is not powered and the VCOIN is typically 3.0V, VCOIN is used for power supply, and the typical power consumption is 2uA

2. 3. Power-up and power-up timing and reset

2. 3. 1. Power-up and power-up timing

VCC33_IO and VDD11_SYS have no power-up and power-up sequencing requirements.

2. 3. 2. Reset the source

The chip system has 7 reset sources, and any of the following reset conditions will reset the chip:

- SYS Power-on Reset: A reset is generated after the VCC33_IO is powered on, and the system automatically releases this reset within 10ms of power-on
- RTC power-on reset: After the RTC is powered on (power source VCC33_IO and VCOIN), the reset is automatically completed
- External Pin Reset: The PIN RESETN input is low and continues to generate a reset for more than 2ms

- Debugger Reset: Generates a reset as soon as the RESET command on the JTAG IO is received
- Watchdog Reset: After the software is enabled, a reset is generated immediately when the WDOG timeout reset condition is satisfied
- Overtemperature Reset: When enabled by software, a reset is generated as soon as the THS temperature exceeds the set value
- Voltage Comparison Reset: Reset occurs immediately when the RTC_IO voltage is higher than the reference voltage (configurable, or when lower than the reference voltage) is enabled by software

2.4. Built-in LDO electrical characteristics

2.4.1. LDO25

Built-in LDO25 with configurable voltage for system simulation and GPADC/eFuse power supply, the electrical characteristics are described below

symbol	description	minimum	Typical	maximum	unit
In	Output voltage	2.4	2.5	3.1	V
This is	Output current	-	-	100	but
Co	External decoupling capacitor	-	1	-	uF

2.4.2. LDO18

The built-in LDO18 voltage is configurable and can be used to power PSRAM IO and PSRAM particles, and its electrical characteristics are described below

symbol	description	minimum	Typical	maximum	unit
In	Output voltage	1.71	1.8	1.92	V
This is	Output current	-	-	100	but
Co	External decoupling capacitor	-	1	-	uF

2.4.3. LDO1x

The built-in LDO1x is voltage configurable and can be used to power VDD11_SYS, and its electrical characteristics are described below

sign	description	minimum	Typical	maximum	unit
In	Output voltage	0.9	1.1	1.9	V
This is	Output current	-	-	500	but
Co	External decoupling capacitor	-	1	-	uF

2.5. clock

2.5.1. External clock source

- The 32.768kHz clock is used for low frequency and RTC.
- A 24.000MHz clock is used to generate a master clock.

symbol	description	minimum	Typical	maximum	unit
OSC_24M	PLL clock source	-	24	-	MHz
OSC_32K	RTC clock source	-	32768	-	Hz

2. 6. IO electrical characteristics

2. 6. 1. IO DC characteristic

sign	description	minimum	Typical	maximum	unit
HIV	High input voltage	0.7*VCC33_IO	-	VCC33_IO+0.3	V
WILL	Low level input voltage	-0.3	-	0.3*VCC33_IO	V
RPU	Pull-up resistor	-	33	-	KΩ
RPD	Pull-down resistors	-	33	-	KΩ
IIH	High input current	-	-	10	U
IIL	Low input current	-	-	10	U
VOH	High output voltage	VCC33_IO-0.3	-	VCC33_IO	V
THEFT	Low level output voltage	0	-	0.3	V
IOH	High-level drive capability	8	-	60	but
IOL	Low-level drive capability	8	-	55	but
IOZ	Three-state output leakage current	-10	-	10	U
CIN	Input capacitance	-	-	5	pF
COST	Output capacitance	-	-	5	pF

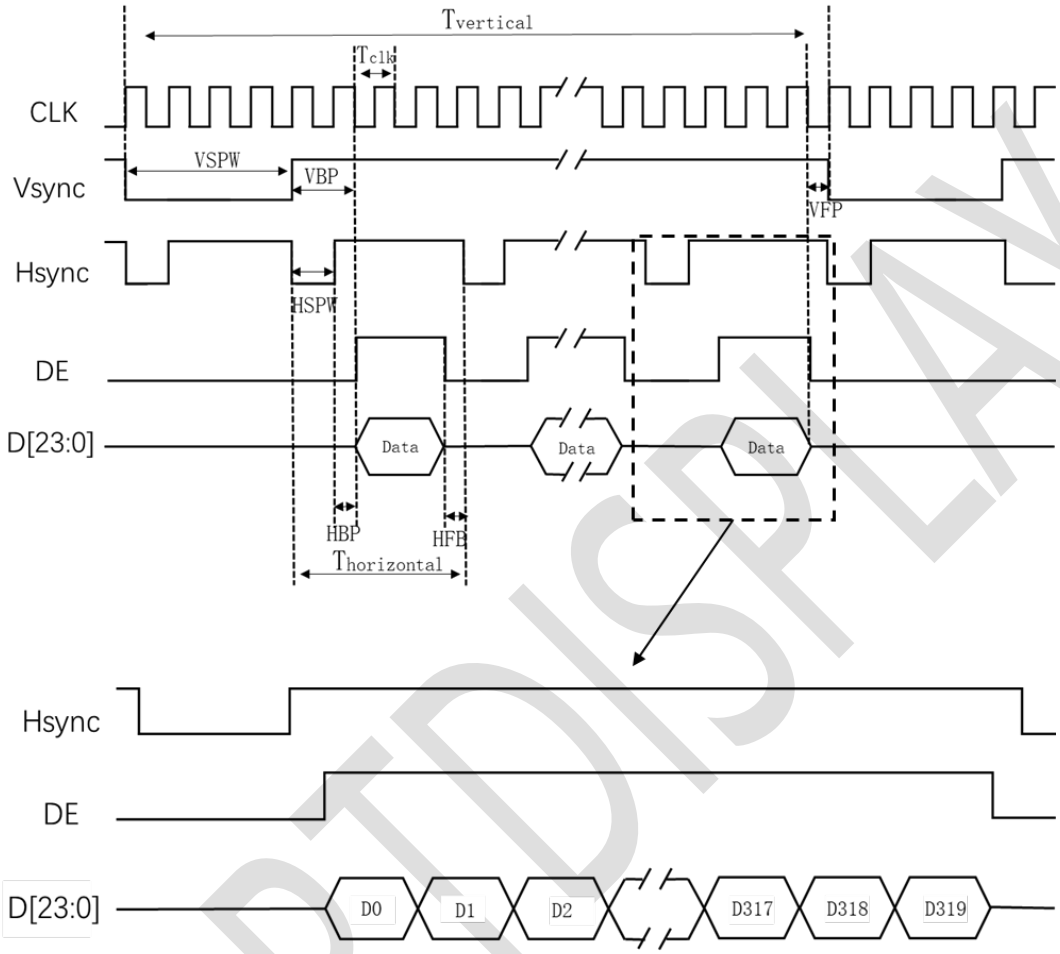
2. 6. 2. IO AC feature

sign	description	Test conditions	minimum	Typical	maximum	unit
fmax	Maximum frequency	Load 6pF	-	-	150	MHz
Tr	Rise time	VOL to VOH time	-	-	1.6	ns
tf	Drop time	VOH to VOL time	-	-	1.6	ns

2. 7. Timing parameters

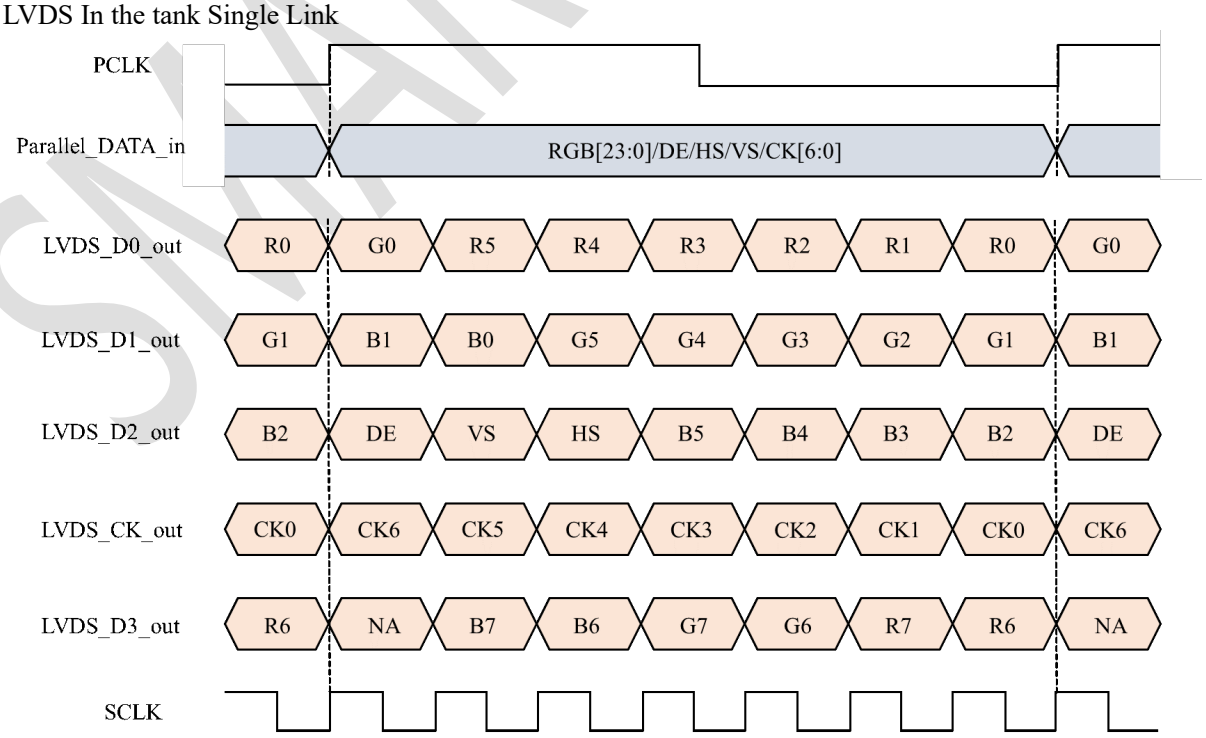
2. 7. 1. Displays the interface timing

2. 7. 1. 1. PRGB timing



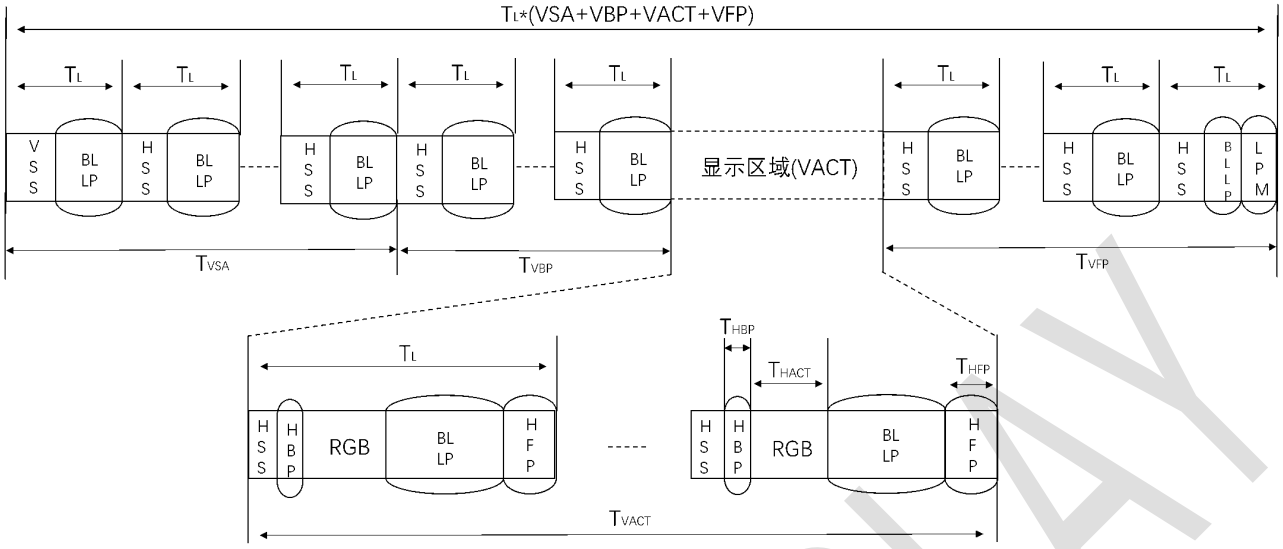
2. 7. 1. 2. LVDS timing

LVDS In the tank Single Link

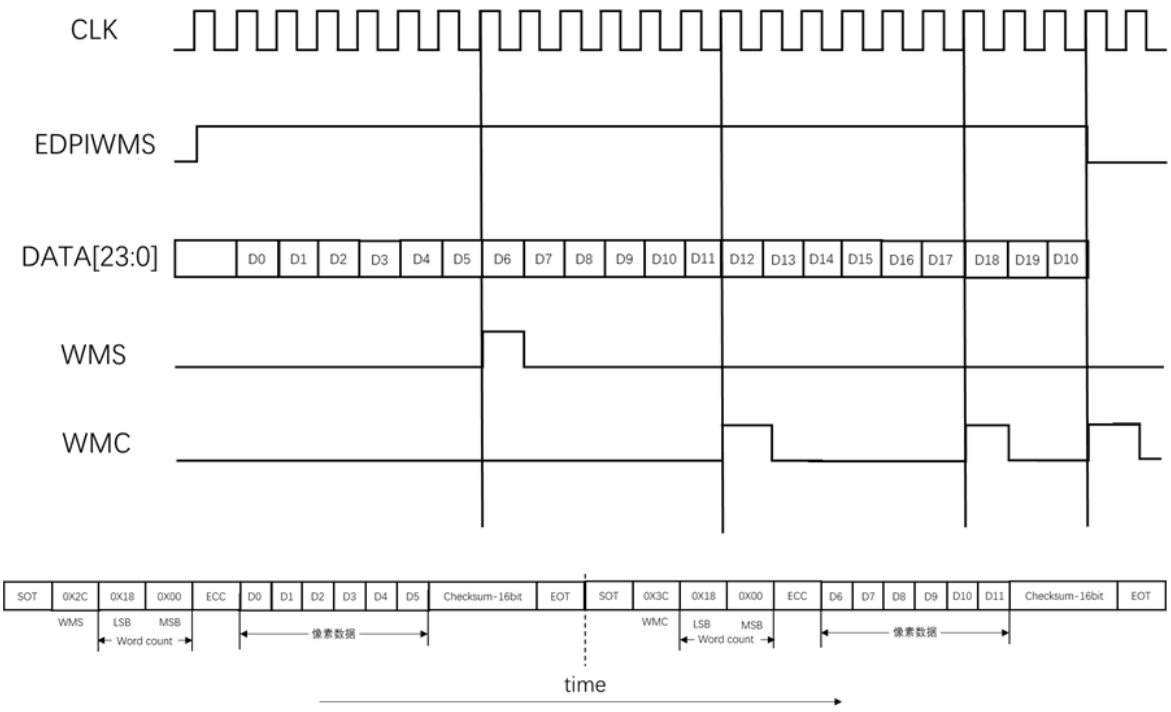


2. 7. 1. 3. MIPI-DSI timing

MIPI-DSI supports Video modes (including Burst mode, Sync Pulse mode, and Sync Event mode).



Video burst 模式

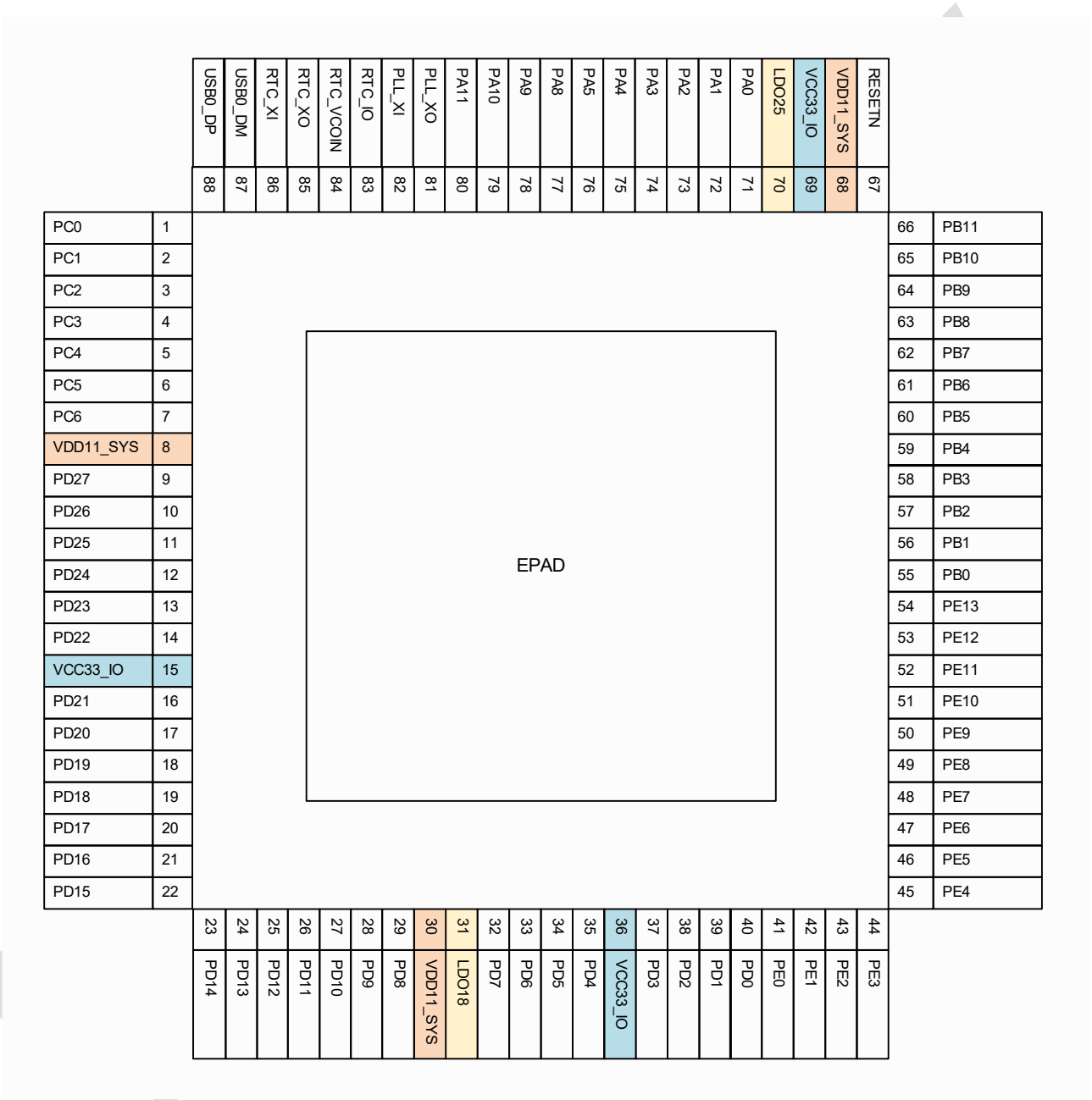


Command Model

3. Package information

3. 1. Pin distribution

3. 1. 1. ZX Model3 QFN88



3. 2. Pin attributes

- [1]: Chip package pin serial number.
- [2]: The name of the chip package pins.
- [3]: Type, indicating the direction of the signal.
  - I – Input;
  - O – output;
  - I/O – Input/Output;
  - OD ——open leakage;
  - A – Simulation;
  - AI – analog input;
  - AO – Analog Output;
  - P – Power supply;
  - G – Ground;
- [4]: Pin reset state, PU refers to pull-up, PD refers to pull-down, Z refers to high-impedance state.
- [5] :P U/PD indicates that there is a pull-up resistor inside and that the pull-up resistor can be turned on or off by software.
- [6]: The default drive capability size. The GPIO has a default drive capability of 20mA and a maximum of 50mA.
- [7]: Power supply.

3. 2. 1. ZX Model3 QFN88

Pin [1]	Name[2]	Type[3]	Reset Status[4]	Pull up and down[5]	Default Driver (mA)[6]	Power Supply [7]
GPIO A						
71	PA0	I/O	With	PU/PD	20	VCC33_IO
72	PA1	I/O	With	PU/PD	20	VCC33_IO
73	PA2	I/O	With	PU/PD	20	VCC33_IO
74	PA3	I/O	With	PU/PD	20	VCC33_IO
75	PA4	I/O	With	PU/PD	20	VCC33_IO
76	PA5	I/O	With	PU/PD	20	VCC33_IO
77	PA8	I/O	PU	PU/PD	20	VCC33_IO
78	PA9	I/O	PU	PU/PD	20	VCC33_IO
79	PA10	I/O	PU	PU/PD	20	VCC33_IO
80	PA11	I/O	PU	PU/PD	20	VCC33_IO
GPIO B						
55	PB0	I/O	With	PU/PD	20	VCC33_IO
56	PB1	I/O	With	PU/PD	20	VCC33_IO
57	PB2	I/O	With	PU/PD	20	VCC33_IO
58	PB3	I/O	With	PU/PD	20	VCC33_IO
59	PB4	I/O	With	PU/PD	20	VCC33_IO
60	PB5	I/O	With	PU/PD	20	VCC33_IO
61	PB6	I/O	With	PU/PD	20	VCC33_IO

62	PB7	I/O	With	PU/PD	20	VCC33_IO
63	PB8	I/O	With	PU/PD	20	VCC33_IO
64	PB9	I/O	With	PU/PD	20	VCC33_IO
65	PB10	I/O	With	PU/PD	20	VCC33_IO
66	PB11	I/O	With	PU/PD	20	VCC33_IO
GPIO C						
1	PC0	I/O	With	PU/PD	20	VCC33_IO
2	PC1	I/O	With	PU/PD	20	VCC33_IO
3	PC2	I/O	With	PU/PD	20	VCC33_IO
4	PC3	I/O	With	PU/PD	20	VCC33_IO
5	PC4	I/O	With	PU/PD	20	VCC33_IO
6	PC5	I/O	With	PU/PD	20	VCC33_IO
7	PC6	I/O	With	PU/PD	20	VCC33_IO
GPIO D						
40	PD0	I/O	With	PU/PD	20	VCC33_IO
39	PD1	I/O	With	PU/PD	20	VCC33_IO
38	PD2	I/O	With	PU/PD	20	VCC33_IO
37	PD3	I/O	With	PU/PD	20	VCC33_IO
35	PD4	I/O	With	PU/PD	20	VCC33_IO
34	PD5	I/O	With	PU/PD	20	VCC33_IO
33	PD6	I/O	With	PU/PD	20	VCC33_IO
32	PD7	I/O	With	PU/PD	20	VCC33_IO
29	PD8	I/O	With	PU/PD	20	VCC33_IO
28	PD9	I/O	With	PU/PD	20	VCC33_IO
27	PD10	I/O	With	PU/PD	20	VCC33_IO
26	PD11	I/O	With	PU/PD	20	VCC33_IO
25	PD12	I/O	With	PU/PD	20	VCC33_IO
24	PD13	I/O	With	PU/PD	20	VCC33_IO
23	PD14	I/O	With	PU/PD	20	VCC33_IO
22	PD15	I/O	With	PU/PD	20	VCC33_IO
21	PD16	I/O	With	PU/PD	20	VCC33_IO
20	PD17	I/O	With	PU/PD	20	VCC33_IO
19	PD18	I/O	With	PU/PD	20	VCC33_IO
18	PD19	I/O	With	PU/PD	20	VCC33_IO
17	PD20	I/O	With	PU/PD	20	VCC33_IO
16	PD21	I/O	With	PU/PD	20	VCC33_IO
14	PD22	I/O	With	PU/PD	20	VCC33_IO

13	PD23	I/O	With	PU/PD	20	VCC33_IO
12	PD24	I/O	With	PU/PD	20	VCC33_IO
11	PD25	I/O	With	PU/PD	20	VCC33_IO
10	PD26	I/O	With	PU/PD	20	VCC33_IO
9	PD27	I/O	With	PU/PD	20	VCC33_IO
GPIO E						
41	PE0	I/O	With	PU/PD	20	VCC33_IO
42	PE1	I/O	With	PU/PD	20	VCC33_IO
43	PE2	I/O	With	PU/PD	20	VCC33_IO
44	PE3	I/O	With	PU/PD	20	VCC33_IO
45	PE4	I/O	With	PU/PD	20	VCC33_IO
46	PE5	I/O	With	PU/PD	20	VCC33_IO
47	PE6	I/O	With	PU/PD	20	VCC33_IO
48	PE7	I/O	With	PU/PD	20	VCC33_IO
49	PE8	I/O	With	PU/PD	20	VCC33_IO
50	PE9	I/O	With	PU/PD	20	VCC33_IO
51	PE10	I/O	With	PU/PD	20	VCC33_IO
52	PE11	I/O	With	PU/PD	20	VCC33_IO
53	PE12	I/O	With	PU/PD	20	VCC33_IO
54	PE13	I/O	With	PU/PD	20	VCC33_IO
RTC						
83	RTC_IO	FROM	-	-	-	-
84	RTC_VCOIN	P	-	-	-	-
85	RTC_XO	Or	-	-	-	-
86	RTC_XI	I	-	-	-	-
PLL						
67	RESETN	I	-	-	-	-
81	PLL_XO	Or	-	-	-	-
82	PLL_XI	I	-	-	-	-
USB						
87	USB_DM	A	-	-	-	-
88	USB_DP	A				
Power						
15,36,69	VCC33_IO	P	-	-	-	-
70	LDO25	P	-	-	-	-
31	LDO18	P	-	-	-	-
8,30,68	VDD11_SYS	P	-	-	-	-

89	GND	P	-	-	-	-

3. 3. Functional reuse

1. ZX Model3 Functional reuse

Table 3.1 Model3 Function Multiplexing Table

Pins	Feature 2	Feature 3	Feature 4	Feature 5	Feature 6	Feature 7	Feature 8
PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX		PSADC0	CPU_NMI
PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX		PSADC1	DE_TE
PA2	GPADC2		I2C1_SCL	UART1_TX		PSADC2	UART2_CTS
PA3	GPADC3		I2C1_SDA	UART1_RX		PSADC3	UART2_RTS
PA4	GPADC4		CAN0_TX	UART2_TX		PSADC4	
PA5	GPADC5		CAN0_RX	UART2_RX		PSADC5	RTC_32K
PA6	GPADC6		CAN1_TX	UART3_TX		PSADC6	
PA7	GPADC7		CAN1_RX	UART3_RX		PSADC7	
PA8	RTP_XP		I2C2_SCL			PSADC8	
PA9	RTP_YP		I2C2_SDA			PSADC9	
PA10	RTP_XN	IR_RX				PSADC10	JTAG_MS
PA11	RTP_YN	IR_TX				PSADC11	JTAG_CK
PB0	SPI0_WP	SPI1_WP		UART4_TX			
PB1	SPI0_MISO	SPI1_MISO		UART6_TX			
PB2	SPI0_CS0	SPI1_CS		UART6_RX			
PB3	SPI0_HOLD	SPI1_HOLD		UART4_RX			
PB4	SPI0_CLK	SPI1_CLK		UART6_RTS			
PB5	SPI0_MOSI	SPI1_MOSI		UART4_RTS	UART6_CTS		
PB6	SDC0_CMD	SPI2_CS		UART5_TX			FLASH_CS
PB7	SDC0_CLK	SPI2_MISO		UART5_RX			FLASH_MISO
PB8	SDC0_D3	SPI2_MOSI		UART5_RTS	UART7_CTS		FLASH_MOSI
PB9	SDC0_D0	SPI2_CLK		UART7_RTS			FLASH_CLK
PB10	SDC0_D1	SPI2_HOLD		UART7_TX			
PB11	SDC0_D2	SPI2_WP	SPI0_CS1	UART7_RX			
PC0	SDC1_D1		I2C2_SCL	UART3_RTS			JTAG_MS
PC1	SDC1_D0						
PC2	SDC1_CLK						UART0_TX
PC3	SDC1_CMD						
PC4	SDC1_D3		I2C1_SCL	UART3_TX			UART0_RX
PC5	SDC1_D2		I2C1_SDA	UART3_RX			JTAG_CK

PC6	SDC1_DET	CAP0	I2C2_SDA	UART3_CTS	DE_TE	CLK_OUT3	
PC7		CAP1					
PC8	SPI3_CLK	CAP2	CAN0_TX	UART4_TX			
PC9	SPI3_CS	CAP3	CAN0_RX	UART4_RX			
PC10	SPI3_MOSI	CAP4	CAN1_TX	UART5_TX			
PC11	SPI3_MISO	CAP5	CAN1_RX	UART5_RX			
PD0	LCD_D0	SPI3_CLK	I2C0_SCL	UART0_TX	PBUS_AD0	EPWM11_B	
PD1	LCD_D1	SPI3_CS	I2C0_SDA	UART0_RX	PBUS_AD1	EPWM11_A	
PD2	LCD_D2	SPI3_MOSI	I2C1_SCL	UART1_TX	PBUS_AD2	EPWM10_B	
PD3	LCD_D3	SPI3_MISO	I2C1_SDA	UART1_RX	PBUS_AD3	EPWM10_A	
PD4	LCD_D4	SPI1_CS	I2C2_SCL	UART2_TX	PBUS_AD4		
PD5	LCD_D5	SPI1_MISO	I2C2_SDA	UART2_RX	PBUS_AD5		
PD6	LCD_D6	SPI1_MOSI	PWM0_A	DSPK0	PBUS_AD6		
PD7	LCD_D7	SPI1_CLK	PWM0_B	DSPK1	PBUS_AD7		
PD8	LCD_D8	SPI1_HOLD	PWM1_A		PBUS_CLK	EPWM9_B	
PD9	LCD_D9	SPI1_WP			PBUS_NCS	EPWM9_A	
PD10	LCD_D10	CAP5			PBUS_NADV	EPWM8_B	
PD11	LCD_D11	CAP4	I2S_DIN		PBUS_NWE	EPWM8_A	
PD12	LCD_D12	CAP3	I2S_DOUT		PBUS_NOE	EPWM7_B	
PD13	LCD_D13	CAP2	I2S_LRCK		CLK_OUT0	EPWM7_A	
PD14	LCD_D14	CAP1	I2S_BCLK		PBUS_AD8	EPWM6_B	
PD15	LCD_D15	CAP0	I2S_MCLK		PBUS_AD9	EPWM6_A	
PD16	LCD_D16	PWM1_B	DMIC_CLK	UART2_TX	PBUS_AD10	EPWM5_B	
PD17	LCD_D17	PWM2_A	DMIC_D0	UART2_RX	PBUS_AD11	EPWM5_A	
PD18	LCD_D18	LVDS_D0N	DSI_D0N		PBUS_AD12	EPWM4_B	
PD19	LCD_D19	LVDS_D0P	DSI_D0P		PBUS_AD13	EPWM4_A	
PD20	LCD_D20	LVDS_D1N	DSI_D1N		PBUS_AD14	EPWM3_B	
PD21	LCD_D21	LVDS_D1P	DSI_D1P		PBUS_AD15	EPWM3_A	
PD22	LCD_D22	LVDS_D2N	DSI_CKN			EPWM2_B	
PD23	LCD_D23	LVDS_D2P	DSI_CKP			EPWM2_A	
PD24	LCD_DCLK	LVDS_CKN	DSI_D2N			EPWM1_B	
PD25	LCD_HS	LVDS_CKP	DSI_D2P		PWM2_B	EPWM1_A	
PD26	LCD_VS	LVDS_D3N	DSI_D3N		PWM3_A	EPWM0_B	
PD27	LCD_DE	LVDS_D3P	DSI_D3P		PWM3_B	EPWM0_A	CMU_CKT
PE0	EMAC_RXD1	DVP_D0	PWM0_A	UART3_TX			
PE1	EMAC_RXD0	DVP_D1	PWM0_B	UART3_RX			
PE2	EMAC_RXCTL	DVP_D2		UART4_TX			

PE3	EMAC_CLKIN	DVP_D3	I2S_MCLK	UART4_RX			
PE4	EMAC_TXD1	DVP_D4		UART5_TX			
PE5	EMAC_TXD0	DVP_D5		UART5_RX			
PE6	EMAC_TXCK	DVP_D6		UART6_TX			
PE7	EMAC_TXCTL	DVP_D7		UART6_RX			
PE8	EMAC_MDC	DVP_CK		UART7_TX			
PE9	EMAC_MDIO	DVP_HS		UART7_RX			
PE10	CLK_OUT2	DVP_VS	I2S_DIN	DMIC_CLK			
PE11	CLK_OUT1	PWM1_A	I2S_LRCK	DMIC_D0			
PE12	SPI2_CLK	PWM1_B	I2S_BCLK	DSPK1			
PE13	SPI2_CS	PWM2_A	I2S_DOUT	DSPK0			
PE14	SPI2_MOSI	I2S_MCLK	I2C0_SCK	UART6_TX			
PE15	SPI2_MISO	PWM2_B	I2C0_SDA	UART6_RX			
PE16	SPI2_HOLD	PWM3_A		UART7_TX			
PE17	SPI2_WP	PWM3_B		UART7_RX			
PU0	USB_DM		UART0_RX	UART1_RX			
PU1	USB_DP		UART0_TX	UART1_TX			

1. ZX Model3 QFN68 Description of the encapsulation pins

Table 34 ZX Model3 QFN88 Package Pin Description

Pins	definition	type	function	Note description
RTC				
83	RTC_IO	FROM	RTC wake-up 32K clock output	OD output, external pull-up resistor is required, and the pull-up voltage cannot exceed 5V
84	RTC_VCOIN	POWER	-	If the power-down can be suspended without
85	RTC_XO	OUTPUT	-	It can be connected to a 32.768kHz passive crystal
86	RTC_XI	INPUT	-	It can be connected to a 32.768kHz passive crystal
SYS				
67	RESETN	INPUT	System reset	Built-in about 30Kohm pull-up resistor and debounce filter, can be directly suspended without use, if the
81	PLL_XO	OUTPUT	-	Connect to 24MHz passive crystal oscillator
82	PLL_XI	INPUT	-	Connect to 24MHz passive crystal oscillator
POWER				
15,36,69	VCC33_IO	POWER	CPU IO voltage	3.3V power supply
70	LDO25	POWER	Built-in LDO output	It is used by the internal analog module and connected to the external 1UF bypass capacitor
31	LDO18	POWER	Built-in LDO output	For internal PSRAM, if used, the chip needs to be cooled, and the external 1uf bypass
8,30,68	VDD11_SYS	POWER	CPU Core Voltage	1.1V power supply, if the built-in LDO1x is used, the

Table 35 D133CB QFN88 Package Function Multiplexing Table

Pins	Feature 1	Feature 2	Feature 3	Feature 4	Feature 5	Feature 6	Feature 8
GPIO A							
71	PA0	GPADC0	IR_TX	I2C0_SCL	UART0_TX		CPU_NMI
72	PA1	GPADC1	IR_RX	I2C0_SDA	UART0_RX		DE_TE
73	PA2	GPADC2		I2C1_SCL	UART1_TX		UART2_CTS
74	PA3	GPADC3		I2C1_SDA	UART1_RX		UART2_RTS
75	PA4	GPADC4		CAN0_TX	UART2_TX		
76	PA5	GPADC5		CAN0_RX	UART2_RX		RTC_32K
77	PA8	RTP_XP		I2C2_SCL			
78	PA9	RTP_YP		I2C2_SDA			
79	PA10	RTP_XN	IR_RX				JTAG_MS
80	PA11	RTP_YN	IR_TX				JTAG_CK
GPIO B							
55	PB0	SPI0_WP	SPI1_WP		UART4_TX		
56	PB1	SPI0_MISO	SPI1_MISO		UART6_TX		
57	PB2	SPI0_CS0	SPI1_CS		UART6_RX		
58	PB3	SPI0_HOLD	SPI1_HOLD		UART4_RX		
59	PB4	SPI0_CLK	SPI1_CLK		UART6_RTS		
60	PB5	SPI0_MOSI	SPI1_MOSI		UART4_RTS	UART6_CTS	
61	PB6	SDC0_CMD	SPI2_CS		UART5_TX		FLASH_CS
62	PB7	SDC0_CLK	SPI2_MISO		UART5_RX		FLASH_MISO
63	PB8	SDC0_D3	SPI2_MOSI		UART5_RTS	UART7_CTS	FLASH_MOSI
64	PB9	SDC0_D0	SPI2_CLK		UART7_RTS		FLASH_CLK
65	PB10	SDC0_D1	SPI2_HOLD		UART7_TX		
66	PB11	SDC0_D2	SPI2_WP	SPI0_CS1	UART7_RX		
GPIO C							
1	PC0	SDC1_D1		I2C2_SCL	UART3_RTS		JTAG_MS
2	PC1	SDC1_D0					
3	PC2	SDC1_CLK					UART0_TX
4	PC3	SDC1_CMD					
5	PC4	SDC1_D3		I2C1_SCL	UART3_TX		UART0_RX
6	PC5	SDC1_D2		I2C1_SDA	UART3_RX		JTAG_CK
7	PC6	SDC1_DET		I2C2_SDA	UART3_CTS	DE_TE	
GPIO D							
40	PD0	LCD_D0	SPI3_CLK	I2C0_SCL	UART0_TX	PBUS_AD0	
39	PD1	LCD_D1	SPI3_CS	I2C0_SDA	UART0_RX	PBUS_AD1	

38	PD2	LCD_D2	SPI3_MOSI	I2C1_SCL	UART1_TX	PBUS_AD2	
37	PD3	LCD_D3	SPI3_MISO	I2C1_SDA	UART1_RX	PBUS_AD3	
35	PD4	LCD_D4	SPI1_CS	I2C2_SCL	UART2_TX	PBUS_AD4	
34	PD5	LCD_D5	SPI1_MISO	I2C2_SDA	UART2_RX	PBUS_AD5	
33	PD6	LCD_D6	SPI1_MOSI	PWM0_A	DSPK0	PBUS_AD6	
32	PD7	LCD_D7	SPI1_CLK	PWM0_B	DSPK1	PBUS_AD7	
29	PD8	LCD_D8	SPI1_HOLD	PWM1_A		PBUS_CLK	
28	PD9	LCD_D9	SPI1_WP			PBUS_NCS	
27	PD10	LCD_D10				PBUS_NADV	
26	PD11	LCD_D11		I2S_DIN		PBUS_NWE	
25	PD12	LCD_D12		I2S_DOUT		PBUS_NOE	
24	PD13	LCD_D13		I2S_LRCK		CLK_OUT0	
23	PD14	LCD_D14		I2S_BCLK		PBUS_AD8	
22	PD15	LCD_D15		I2S_MCLK		PBUS_AD9	
21	PD16	LCD_D16	PWM1_B	DMIC_CLK	UART2_TX	PBUS_AD10	
20	PD17	LCD_D17	PWM2_A	DMIC_D0	UART2_RX	PBUS_AD11	
19	PD18	LCD_D18	LVDS_D0N	DSI_D0N		PBUS_AD12	
18	PD19	LCD_D19	LVDS_D0P	DSI_D0P		PBUS_AD13	
17	PD20	LCD_D20	LVDS_D1N	DSI_D1N		PBUS_AD14	
16	PD21	LCD_D21	LVDS_D1P	DSI_D1P		PBUS_AD15	
14	PD22	LCD_D22	LVDS_D2N	DSI_CKN			
13	PD23	LCD_D23	LVDS_D2P	DSI_CKP			
12	PD24	LCD_DCLK	LVDS_CKN	DSI_D2N			
11	PD25	LCD_HS	LVDS_CKP	DSI_D2P		PWM2_B	
10	PD26	LCD_VS	LVDS_D3N	DSI_D3N		PWM3_A	
9	PD27	LCD_DE	LVDS_D3P	DSI_D3P		PWM3_B	CMU_CKT
GPIO E							
41	PE0	EMAC_RXD1	DVP_D0	PWM0_A	UART3_TX		
42	PE1	EMAC_RXD0	DVP_D1	PWM0_B	UART3_RX		
43	PE2	EMAC_RXCTL	DVP_D2		UART4_TX		
44	PE3	EMAC_CLKIN	DVP_D3	I2S_MCLK	UART4_RX		
45	PE4	EMAC_TXD1	DVP_D4		UART5_TX		
46	PE5	EMAC_TXD0	DVP_D5		UART5_RX		
47	PE6	EMAC_TXCK	DVP_D6		UART6_TX		
48	PE7	EMAC_TXCTL	DVP_D7		UART6_RX		
49	PE8	EMAC_MDC	DVP_CK		UART7_TX		
50	PE9	EMAC_MDIO	DVP_HS		UART7_RX		

51	PE10	CLK_OUT2	DVP_VS	I2S_DIN	DMIC_CLK		
52	PE11	CLK_OUT1	PWM1_A	I2S_LRCK	DMIC_D0		
53	PE12	SPI2_CLK	PWM1_B	I2S_BCLK	DSPK1		
54	PE13	SPI2_CS	PWM2_A	I2S_DOUT	DSPK0		
USB							
87	PU0	USB_DM		UART0_RX	UART1_RX		
88	PU1	USB_DP		UART0_TX	UART1_TX		

3. 4. Pin/Signal Description

Pin/signal name	description	type
SYSTEM		
RESETN	Reset the pins	I
PLL_XI	24MHz crystal input	TO
PLL_XO	24MHz crystal output	TO
RTC		
RTC_IO	RTC wake-up output	FROM
RTC_VCOIN	RTC coin cell battery powered	P
RTC_XO	32.768Khej Crystal output	TO
RTC_XI	32.768KHz crystal input	TO
USB		
USB_DM	Negative end of the USB data signal	AI/O
USB_DP	USB data signal positive end	AI/O
RTP		
RTP_XP	RTP X direction is positive	TO
RTP_YP	RTP Y direction is positive	TO
RTP_XN	RTP X direction negative end	TO
RTP_YN	RTP Y direction negative end	TO
ADC,x = 0~5		
GPADCx	Analog sample signal input	TO
GPADCx	Analog sample signal input	TO
EMAC		
EMAC_RXD1	RMII Data Receive Signal Line 1	I
EMAC_RXD0	RMII Data Receive Signal Line 0	I
EMAC_RXCTL	RMII data reception is valid	I
EMAC_CLKIN	RMII Reference Clock	I
EMAC_TXD1	RMII Data Transmit Signal Cable 1	Or

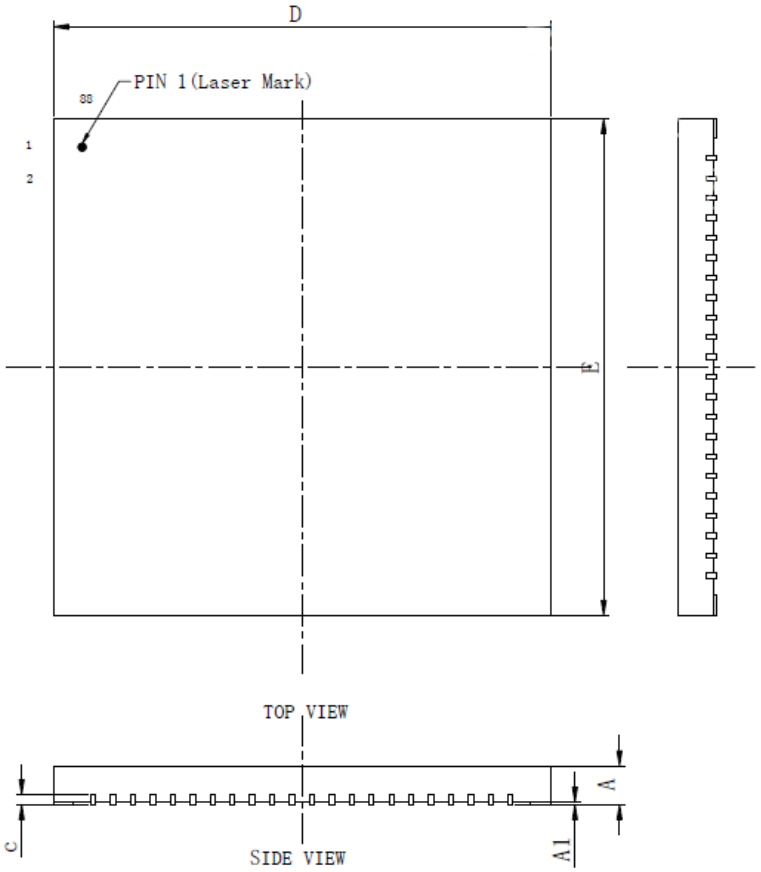
EMAC_TXD0	RMII Data Transmit Signal Cable 0	Or
EMAC_TXCK	RMII sends the clock	Or
EMAC_TXCTL	RMII data transmission enabled	Or
EMAC_MDC	RMII Serial Management Interface Clock	I/O
EMAC_MDIO	RMII Serial Management Interface Data	I/O
CLK_OUTx	Configurable 25MHz clock output, x = 0~3	Or
PWM,x = 0~3		
PWMx_A	PWMx A channel	Or
PWMx_B	PWMx B channel	Or
SPI,x = 0~3		
SPIx_HOLD	SPIx holds the signal and is active low	I/O
SPIx_WP	SPIx write-protected signal, active-low	I/O
SPIx_CS	SPIx Chip selected signal, active low	I/O
SPIx_CLK	SPIx clock signal	I/O
SPIx_MOSI	SPIx master data output, slave data input	I/O
SPIx_MISO	SPIx master data input, slave data output	I/O
UART,x = 0~7		
UARTx_TX	UARTx data sending	Or
UARTx_RX	UARTx data reception	I
UARTx_CTS	UARTx sends allowed	I
UARTx_RTS	UARTx sends the request	Or
I2C,x = 0~2		
I2Cx_SCL	I2Cx serial clock signal	I/O
I2Cx_SDA	I2Cx serial data signal	I/O
CAN		
CAN0_TX	CAN0 data transmission, external CAN bus transceiver	Or
CAN0_RX	CAN0 data reception, external CAN bus transceiver	I
CAN1_TX	CAN1 data transmission, external CAN bus transceiver	Or
CAN1_RX	CAN1 data reception, external CAN bus transceiver	I
CIR		
IR_TX	Infrared data sending	Or
IR_RX	Infrared data reception	I
I2S		
I2S_MCLK	I2Sx Master Clock	Or
I2S_LRCK	I2Sx Left/Right Clock	I/O
I2S_BCLK	I2Sx bit clock	I/O
I2S_DOUT	I2Sx serial data output	Or

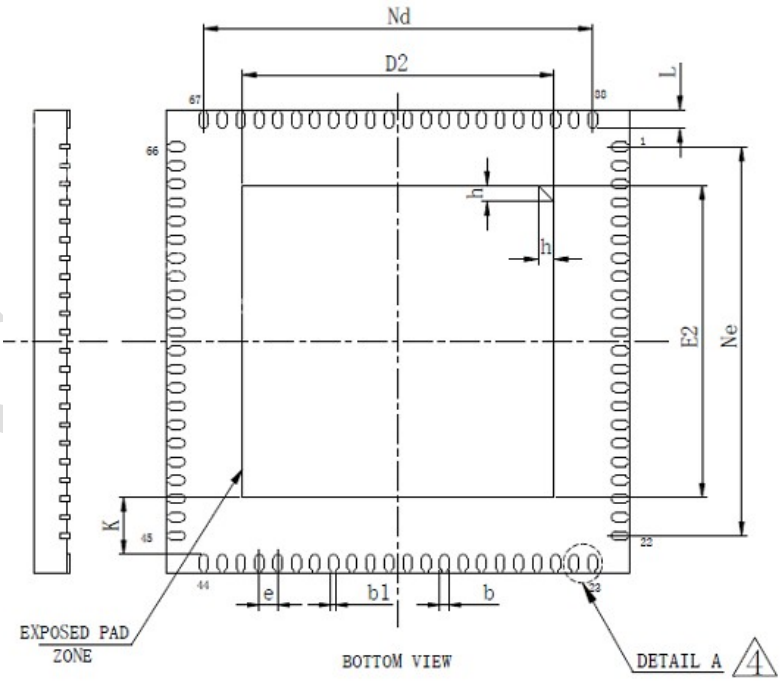
I2S_DIN	I2Sx serial data entry	I
DSPK		
DSPK0	Speaker Signal output channel 0	I/O
DSPK1	Speaker Signal output channel 1	I/O
DMIC		
DMIC_CLK	PDM digital microphone clock signal	Or
DMIC_D0	PDM digital microphone data signal	I/O
SDC,x = 0~1		
SDCx_CMD	SDC0 control signal	I/O
SDCx_CLK	SDC0 clock signal	Or
SDCx_D[3:0]	SDC0 data input and output	I/O
LCD		
LCD_D[23:0]	LCD data output	Or
LCD_DCLK	LCD clock signal	Or
LCD_HS	LCD line field synchronization	Or
LCD_VS	LCD field synchronization	Or
LCD_DE	LCD data enabled	Or
LVDS		
LVDS_CKN	LVDSx Clock Negative	TO
LVDS_CKP	LVDSx clock head	TO
LVDS_D0N	LVDSx data 0 negative end	TO
LVDS_D0P	LVDSx data 0 is at the positive end	TO
LVDS_D1N	LVDSx data 1 negative end	TO
LVDS_D1P	LVDSx data 1 is at the positive end	TO
LVDS_D2N	LVDSx data 2 negative end	TO
LVDS_D2P	LVDSx Data 2 Positive	TO
LVDS_D3N	LVDSx data 3 negative end	TO
LVDS_D3P	LVDSx data 3 is positive	TO
MIPI CIO		
DSI_CKN	MIPI DSI Negative end of the clock	TO
DSI_CKP	MIPI DSI The clock is at the right end	TO
DSI_D0N	MIPI DSI data 0 negative end	AI/O
DSI_D0P	MIPI DSI data 0 is positive	AI/O
DSI_D1N	MIPI DSI data 1 negative end	AI/O
DSI_D1P	MIPI DSI data 1 is positive	AI/O
DSI_D2N	MIPI DSI data 2 negative end	AI/O
DSI_D2P	MIPI DSI data 2 is positive	AI/O

DSI_D3N	MIPI DSI data 3 negative end	AI/O
DSI_D3P	MIPI DSI data 3 is positive	AI/O
DVP		
DVP_CK	DVP pixel clock	I
DVP_HS	DVP line field synchronization	I
DVP_VS	DVP column field synchronization	I
DVP_D[7:0]	DVP data entry	I

3. 5. Package size

3. 5. 1. ZX Model3 QFN88





SYMBOL	MILLIMETER			
	MIN	NOM	MAX	
A	0. 70	0. 75	0. 80	3
	0. 80	0. 85	0. 90	
	0. 85	0. 90	0. 95	4
A1	0	0. 02	0. 05	
b	0. 15	0. 20	0. 25	
b1	0. 10REF			5
c	0. 18	0. 20	0. 25	
D	9. 90	10. 00	10. 10	
D2	6. 64	6. 74	6. 84	
e	0. 40BSC			
Nd	8. 40REF			
E	9. 90	10. 00	10. 10	
E2	6. 64	6. 74	6. 84	
Ne	8. 40REF			
L	0. 30	0. 40	0. 50	
K	0. 20	-	-	
h	0. 30	0. 35	0. 40	